In the Specification:

Please replace all references from attorney docket number "121744-0003 (CIT 3190-1)" to – CIT 3190-1--

Please replace paragraph [0019] with the following amended paragraph:

[0019] In this more detailed embodiment, the ~~downconverterfurther~~ **downconverter further** includes a first summing circuit that sums the outputs of the first and second mixers, a second summer that sums the outputs of the fifth and sixth mixers, a third summing circuit that sums the outputs of the third and fourth mixers, and a fourth summing circuit that sums the outputs of the seventh and eighth mixers.

Please replace paragraph [0075] with the following amended paragraph:

[0075] However, in the preferred embodiment shown in FIG. 8, each of the four IF mixing stages includes an additional mixer to mix the various combinations of in-phase and quadarature signals. By properly combining (add/subtract) these [[**mized**]] **mixed** signals, not only are quadrature signals at baseband provided, but ~~improed~~ **improved** image rejection is also achieved. As disclosed by Crols and Steyaert in "A Single-Chip 900 MHz CMOS Receiver Front-End With A High Performance Low-IF Topology," IEEE Journal of Solid-State Circuits, Vol. 30, No. 12, December 1995, this technique is known in the art as double quadrature downconversion. In particular, mixing stage 460 includes a fifth mixer 464 that mixes f.sub.LO2Q with IF.sub.I and mixing stage 470 includes a sixth mixer 474 that mixes f.sub.LO2I with IF.sub.Q. The outputs of these mixers 464 and 474 are combined at summing circuit 496 to produce a first quadrature baseband signal, denoted as BB,Q.sub.A. Moreover, mixing stage 480 includes a seventh mixer 484 that mixes f.sub.LO3Q with IF.sub.1 and mixing stage 490 includes an eighth mixer 494 that mixes f.sub.LO3I with IF.sub.Q. The outputs of these mixers, 484 and 494 are combined at summing circuit 498 to produce a second quadrature baseband signal, denoted as BB,Q.sub.B.